UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/730,039	12/05/2000	Moataz A. Mohamed	00CON102P	6842

25700 7590 05/17/2005

FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 05/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/730,039	MOHAMED ET AL.	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,11-15 and 21-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9, 11-15, and 21-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-9, 11-15, and 21-28 have been considered. Claims 1, 9, and 21 have been amended as per Applicant's request. Claims 16-20 have been cancelled as per Applicant's request.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-9 and 11-28 are rejected under 35 U.S.C. 102(e) as being taught by Tremblay et al., U.S. Patent Number 6,615,338 (herein referred to as Tremblay).

4. Referring to claim 1, Tremblay has taught a processor comprising:

   a. A first plurality of threads, each of said first plurality of threads comprising one of a second plurality of processing units (Tremblay Abstract, lines 1-3 and 11-18; column 3, lines 15-18; column 5, line 64 to column 6, line 14; column 6, line 51 to column 7, line 6; Figure 2; and Figure 3);

   b. A fourth plurality of instruction packets, wherein each of said fourth plurality of instruction packets comprises a third plurality of issue groups (Tremblay Abstract, lines 1-3 and 11-18; column 1, line 58 to column 2, line 8; column 14, lines 53-61; and Figure 10A);

c. Each of said issue groups requiring an internal instruction bus no greater than 64 bits wide for transport to one of said processing units (Tremblay column 1, line 58 to column 2, line 5 and Figure 3, connections between 225 and 220);

d. Each of said first plurality of threads receiving a respective one of said third plurality of issue groups from a respective one of said fourth plurality of instruction packets (Tremblay Abstract, lines 1-3 and 11-18; column 5, line 64 to column 6, line 14; column 6, line 51 to column 7, line 6; and Figure 3); and

e. A respective one of said second plurality of processing units executing said third plurality of issue groups in a single clock cycle, wherein at least two issue groups of said third plurality of issue groups are from different instruction packets of said fourth plurality of instruction packets (Tremblay Abstract, lines 1-3 and 11-18; column 1, line 58 to column 2, line 8; column 3, lines 15-18; column 5, line 64 to column 6, line 14; column 6, line 51 to column 7, line 6; column 14, lines 53-61; Figure 3; and Figure 10A).

5. Referring to claim 9, Tremblay has taught a method for improving performance of a VLIW processor comprising:

a. Dividing a first instruction packet into a first packet first issue group and a first packet second issue group (Tremblay Abstract, lines 1-3 and 11-18; column 1, line 58 to column 2, line 8; column 14, lines 53-61; and Figure 10A);

b. Dividing a second instruction packet into a second packet first issue group and a second packet second issue group (Tremblay Abstract, lines 1-3 and 11-18; column 1, line 58 to column 2, line 8; column 14, lines 53-61; and Figure 10A);

c. Providing, through a first internal instruction bus no greater than 64 bits wide (Tremblay column 1, line 58 to column 2, line 5 and Figure 3, connections between 225 and 220), said first packet first issue group to a first thread having a first thread processing unit and, through a second internal instruction bus no greater than 64 bits wide (Tremblay column 1, line 58 to column 2, line 5 and Figure 3, connections between 225 and 220), said second packet first issue group to a second thread having a second thread processing unit during a first clock cycle (Tremblay Abstract, lines 1-3 and 11-18; column 3, lines 15-18; column 5, line 64 to column 6, line 14; column 6, line 51 to column 7, line 6; Figure 2; and Figure 3); and

d. Providing, through said first internal instruction bus (Tremblay column 1, line 58 to column 2, line 5 and Figure 3, connections between 225 and 220), said first packet second issue group to said first thread having said first thread processing unit and, through said second internal instruction bus (Tremblay column 1, line 58 to column 2, line 5 and Figure 3, connections between 225 and 220), said second packet second issue group to said second thread having said second thread processing unit during a second clock cycle, wherein said first instruction packet is a different instruction packet than said second instruction packet (Tremblay Abstract, lines 1-3 and 11-18; column 1, line 58 to column 2, line 8; column 3, lines 15-18; column 5, line 64 to column 6, line 14; column 6, line 51 to column 7, line 6; column 14, lines 53-61; Figure 3; and Figure 10A).

6. Referring to claim 21, Tremblay has taught a method for improving performance of a VLIW processor comprising:

a. Dividing each one of a first plurality of instruction packets into a second plurality of issue groups (Tremblay Abstract, lines 1-3 and 11-18; column 1, line 58 to column 2, line 8; column 14, lines 53-61; and Figure 10A)

b. Providing each one of said second plurality of issue groups in one of a third plurality of clock cycles, to a respective thread having a respective processing unit (Tremblay Abstract, lines 1-3 and 11-18; column 3, lines 15-18; column 5, line 64 to column 6, line 14; column 6, line 51 to column 7, line 6; Figure 2; and Figure 3);

c. Each of said issue groups requiring an internal instruction bus no greater than 64 bits wide for transport to one of said processing units (Tremblay column 1, line 58 to column 2, line 5 and Figure 3, connections between 225 and 220);

d. Executing said first plurality of instruction packets in said third plurality of clock cycles, wherein an issue group from each one of said first plurality of instruction packets is executed in one of said third plurality of clock cycles, wherein at least two issue groups of said second plurality of issue groups are from different instruction packets of said first plurality of instruction packets (Tremblay Abstract, lines 1-3 and 11-18; column 1, line 58 to column 2, line 8; column 3, lines 15-18; column 5, line 64 to column 6, line 14; column 6, line 51 to column 7, line 6; column 14, lines 53-61; Figure 3; and Figure 10A).

7. Referring to claims 2 and 22, Tremblay has taught wherein each of said first, second, third, and fourth pluralities is equal to two (Tremblay column 1, line 58 to column 2, line 8; column 6, lines 3-5; and column 22, line 61 to column 23, line 13).

8. Referring to claims 3 and 23, Tremblay has taught wherein each of said fourth plurality of instruction packets comprises two issue groups (Tremblay column 1, line 58 to column 2, line 8; column 5, line 64 to column 6, line 14; and column 7, lines 55-62).\

9. Referring to claims 4, 11, and 24, Tremblay has taught wherein each of said fourth plurality of instruction packets is 128 bits wide (Tremblay column 1, line 58 to column 2, line 5).

10. Referring to claims 5, 12, and 25, Tremblay has taught wherein a first one of said two issue groups is 64 bits wide and a second one of said two issue groups is 48 bits wide (Tremblay column 1, line 58 to column 2, line 5).

11. Referring to claims 6, 13, and 26, Tremblay has taught wherein a first one of said two issue groups is 48 bits wide and a second one of said two issue groups is 64 bits wide (Tremblay column 1, line 58 to column 2, line 5).

12. Referring to claims 7 and 27, Tremblay has taught wherein each of said fourth plurality of instruction packets resides in a respective instruction cache and is addressed by a respective program counter (Tremblay column 1, line 58 to column 2, line 5).

13. Referring to claim 8, Tremblay has taught wherein each of said first, second, third, and fourth pluralities is equal to four (Tremblay column 1, line 58 to column 2, line 5).

14. Referring to claim 14, Tremblay has taught wherein said second packet first issue group comprises 64 bits and said second packet second issue group comprises 48 bits (Tremblay column 1, line 58 to column 2, line 5).

15. Referring to claim 15, Tremblay has taught wherein said second packet first issue group comprises 48 bits and said second packet second issue group comprises 64 bits (Tremblay column 1, line 58 to column 2, line 5).

16. Referring to claim 28, Tremblay has taught wherein said first plurality is equal to four, and wherein each of said second and third pluralities is equal to two (Tremblay column 1, line 58 to column 2, line 8; column 6, lines 3-5; and column 22, line 61 to column 23, line 13).

Response to Arguments

17. Applicant's arguments filed 24 February 2005 have been fully considered but they are not persuasive. Applicant's argue in essence on pages 8-11

> ...Tremblay does not disclose or even suggest a busing architecture for reducing the width of instruction buses, as disclosed and claimed by amended independent claims of the present invention. In other words, Tremblay does not disclose or suggest a busing architecture with internal instruction buses no greater than 64 bits wide for transport of issue groups to each thread of the VLIW processor.

18. This has not been found persuasive. The added claim limitation states "each of said issue groups requiring an **internal instruction bus** no greater than 64 bits wide for transport to one of **said processing units**" or something similar in scope. When read in the broadest reasonable interpretation, the issue group requires, at most, a bus 64 bits wide to be communicated to a processing unit, so the bus into a processing unit needs not be larger than 64 bits. Tremblay shows a bus connecting the pipeline control unit (PCU) 226 that controls transfer of the instructions to the functional, i.e. processing, units (Tremblay column 7, lines 30-38). Tremblay teaches in column 1, line 64 to column 2, line 5 that a VLIW instruction has a set of fields, called

subinstructions, that correspond to a functional unit, i.e. an issue group for each processing unit, that typically range from 16 to 64 bits in size per functional unit. This means that the bus transporting a subinstruction, i.e. issue group, to a functional unit, i.e. processing unit, needs to be, at maximum, 64 bits wide. Therefore, Tremblay has taught the newly added limitation to the independent claims.

Conclusion

19. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 7 CFR 1.136(a).

20. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

22. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

23. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
12 May 2005

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100